



Audio/Video Module

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1.0 Introduction

The Audio/Video Module (A/V Board) is a component of Avnet Avenue Solutions that will interface, via a standard AvBus connector, to other Avalon components capable of hosting the A/V Board. This document describes the functionality, interfaces, and usage of the A/V Board.

1.1 Description

The Audio/Video (A/V) Module is not a stand-alone module; it is intended to be hosted by an entity with sufficient capability to utilize the audio/video features and provide whatever intermediate processing is required. In its intended role, the A/V Module will capture analog audio, and analog baseband video, convert them to digital and furnish these data, via an AvBus connector, to the Host entity. Additionally, the A/V Module will capture digital camera video via an ITU-R BT.656 interface and furnish these data to the Host via the AvBus connector. The Host will provide whatever processing is required (e.g., video upsampling/downsampling, color-space conversion, etc.) and furnish this manipulated data, along with any other required signals (e.g., synchronization) to the A/V Module via the AvBus.

While any Avalon main board component with sufficient processing power and control flexibility may host the A/V Module, this document assumes an FPGA host and is structured accordingly. The A/V Module will be controlled by, and interact with, an Avnet Host FPGA board via a standard AvBus connector. The A/V Module will provide interfaces to accommodate RGB monitors, an LCD panel, standard definition television monitors, standard video cameras, and BT.656-compatible CCD cameras. The A/V Module provides the ability to capture composite video as well as CIF-resolution non-interlaced video. An audio CODEC is provided to facilitate audio processing; but no mechanism for audio/video synchronization exists; the host must provide this if it is required. In addition, a PS2 keyboard and mouse interface is provided as well as a touchscreen controller. The A/V Board is powered by +3.3V supplied by the AvBus connector. A block diagram of the A/V Module and its interfaces is shown in Figure 1. Figure 2 depicts the A/V Board mated to the Virtex-II Development Board and shows processing that might be utilized. Figure 3 is a photo of the A/V Board.

Demonstration VHDL code is available via download to configure the I2C and AC97 devices on the A/V Module and to exercise these devices.

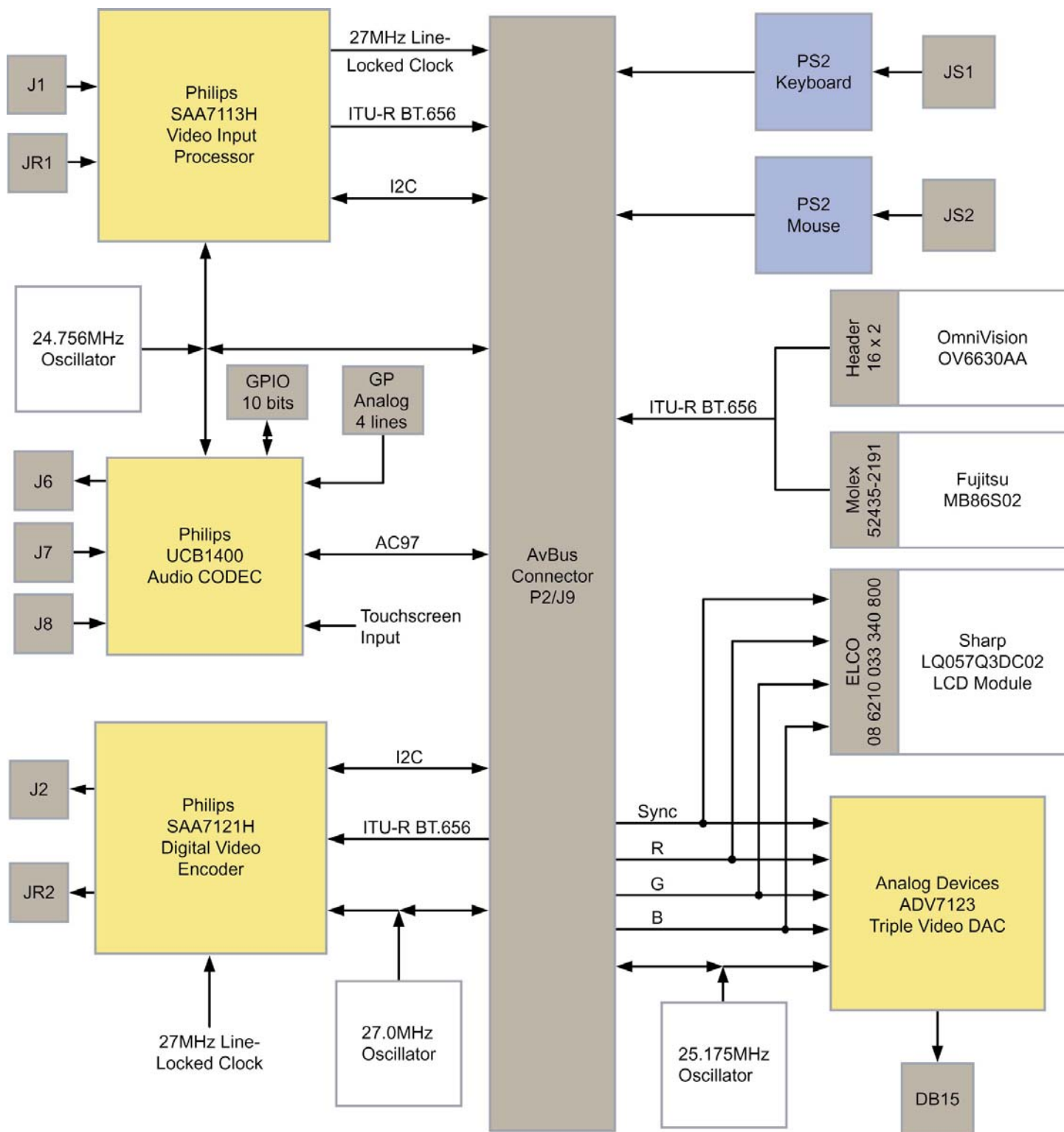


Figure 1: A/V Module Block Diagram

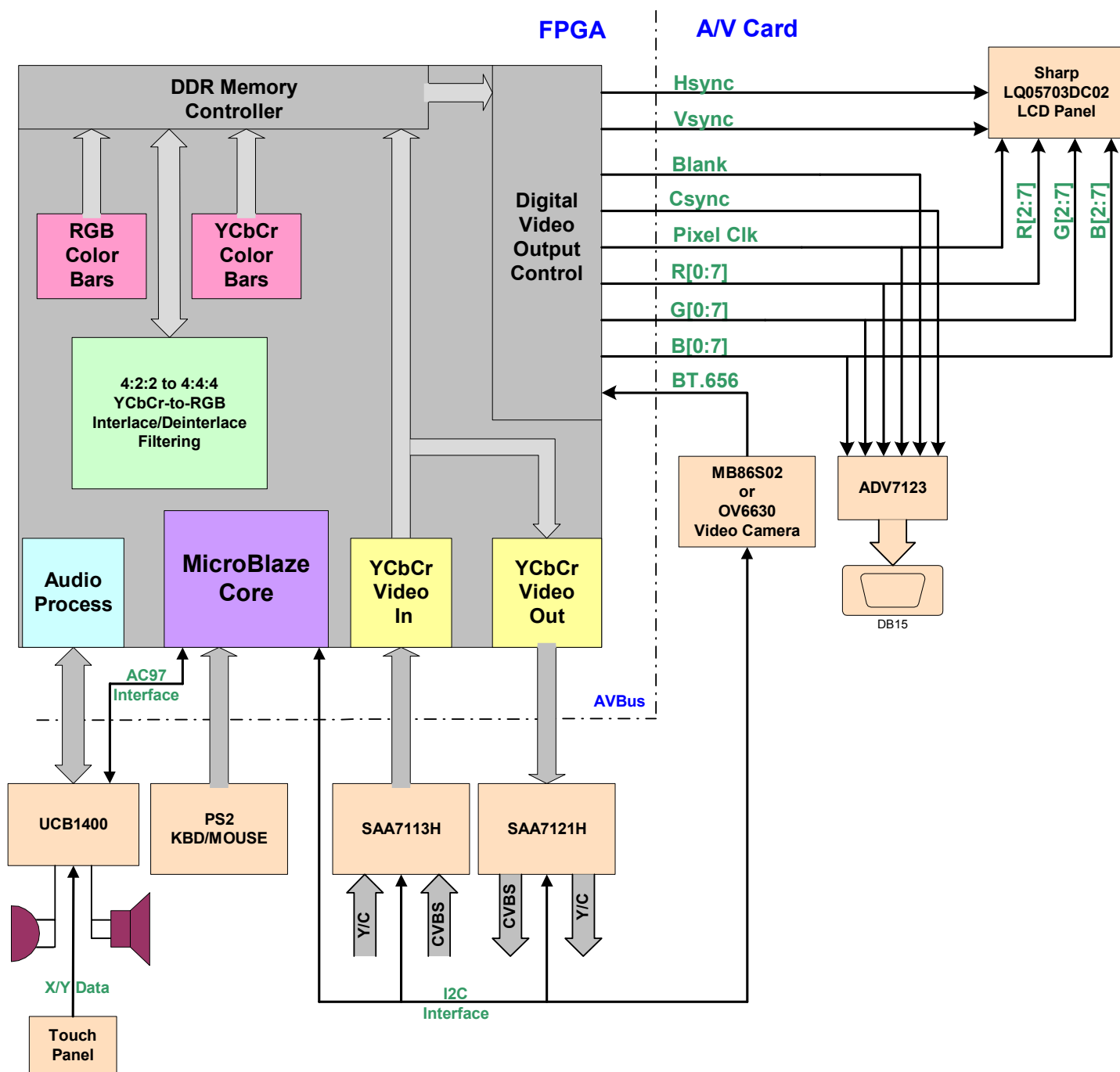


Figure 2: System Block Diagram

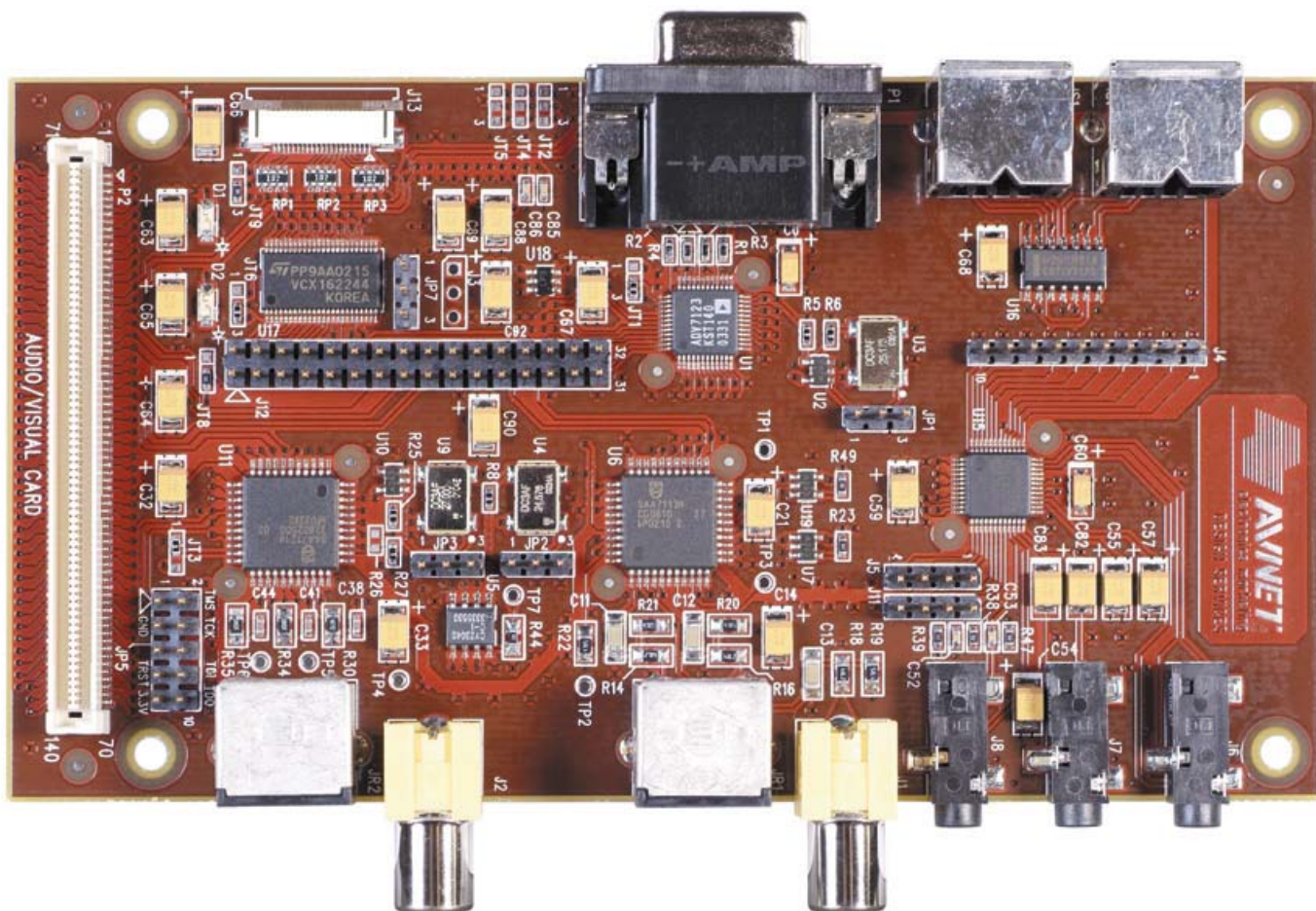


Figure 3: Audio/Video Module

1.2 Features

- Philips SAA7113H Enhanced Video Input Processor for video capture
- Philips SAA7121H Digital Video Encoder for baseband composite video encoding
- Philips UCB1400 20-bit audio CODEC for high-quality audio capture and encoding
- Analog Devices ADV7123 triple high-speed video DAC for analog RGB encoding
- Connectors for:
 - Fujitsu MB86S02 CIF-resolution video camera
 - OmniVision OV6630AA CIF-resolution video camera module
 - Sharp LQ057Q3DC02 Color TFT LCD Module
 - Composite and S-Video in/out
 - Stereo audio in/out
 - Microphone in
- X/Y Touchscreen Controller (via UCB1400)
- PS2 keyboard and mouse interfaces

1.3 Demo Applications

The following VHDL applications may be downloaded:

- Color bars to an RGB monitor (640 X 480 resolution) via the ADV7123.
- Baseband video captured via SAA7113H (ITU-R BT.656) and passed through the FPGA to the SAA7121H for encoding to baseband composite video.
- Audio captured (A/D) by the UCB1400 and encoded (D/A) for output.

These applications include VHDL code to configure the SAA7113H and SAA7121H via I²C and the UCB1400 via AC97.

1.4 Ordering Information:

The following table lists the (eval/dev) system part numbers and available software options.
Internet link at www.em.avnet.com/ads

Part Number	Hardware
ADS-AV-DAU	Audio/Video Module

Table 1: Ordering Information

2.0 Related Documents

The devices referenced by the documents listed below comprise the majority of the A/V Board functionality.

- a) Analog Devices ADV7123 triple video DAC Data Sheet
- b) Philips SAA7121 Digital Video Encoder Data Sheet
- c) Philips SAA7113H Video Input Processor
- d) Philips UCB1400 AC97 CODEC Data Sheet
- e) OmniVision OV6630 CIF CMOS Color Digital Camera Data Sheet
- f) Fujitsu MB86S02 CIF CMOS Color Digital Camera Data Sheet
- g) Sharp LQ057Q3DC02 Color TFT LCD Module Data Sheet
- h) ERG 8M052322 DC to AC Inverter Data Sheet
- i) Rec. ITU-R BT.470-6 Conventional Television Systems
- j) Rec. ITU-R BT.656: Interfaces for Digital Component Video Signals in 525-line and 625-line television systems operating at the 4:2:2 level of recommendation ITU-R BT.601 (Part A)
- k) Rec. ITU-R BT.601: Studio Encoding of Parameters of Digital Television for Standard 4:3 and Wide-Screen 16:9 Aspect Ratio
- l) ANSI/SMPTE 125-1995 Component Video Signal 4:2:2 bit-parallel digital interface
- m) SMPTE 170M-1999 Composite Analog Video Signal
- n) A/V Module Schematics

3.0 A/V Module Description

As shown in Figures 1 and 2, the A/V Module contains only input and output interface devices, and depends on an intelligent Host to control and utilize these interfaces. Interface with the Host entity is provided by AvBus connectors P2 (top) and J9 (bottom). The P2/J9 connector pair signals are paralleled, allowing the A/V Module to plug into its host from the top or bottom as required. Details of the various devices that comprise the A/V Board functionality are provided below. Pin allocation of the P2/J9 connector-pair is listed in Tables A-1 and A-2.

3.1 Video Input Processing

The A/V Module provides three video input options; a Philips SAA7113H Video Input Processor which will capture video from a standard video camera (NTSC baseband composite or S-video (Y/C)), An OmniVision OV6630AA CIF-resolution camera module (via J12), or a Fujitsu MB86S02 CIF-resolution camera module (via J13). These inputs are described below. Note that the OV6630 and the MB86S02 are mutually-exclusive; either may be used but only one may be connected at a time; three-pad zero-ohm jumpers on the A/V Module must be set accordingly:

Jumper Settings for OV6630:

JT6:	2:3
JT7:	1:2
JT8:	1:2
JT9:	2:3

Jumper Settings for MB86S02:

JT6:	1:2
JT7:	1:2
JT8:	2:3
JT9:	1:2

3.1.1 Philips SAA7113H Video Input Processor

A Philips SAA7113H Video Input Processor provides a video capture capability, converting analog composite (CVBS) or Y/C (S) video to digital format. The Host module must establish the operating configuration of this device via an I2C bus interface prior to operation. This device will accept either a CVBS (J1) or Y/C (JR1) signal from an external analog video source and convert that video to a digital format. A 24.576MHz oscillator provides the required clocking for the SAA7113H; this clock is also furnished to the AvBus connector for use by the host, and to the audio CODEC. This 24.576MHz clock is converted to 27.0MHz internal to the SAA7113H and synchronizes output on the Vin_VPO[0:7] data bus.

The 75-ohm CVBS (J1) and Y/C (JR1) inputs are AC-coupled to the SAA7113H. External anti-aliasing filters are not required as these are contained on-chip. The CVBS input is connected to SAA7113H port AI11; see SAA713H data sheet Figure 35 which depicts Mode 0; CVBS – automatic gain. The S-video (Y/C) input is connected to SAA7113H port AI12 (Y) and AI22 (C); see SAA713H data sheet Figure 42 which depicts Mode 9; Y – automatic gain, + C – gain channel 2 adapted to Y gain.

Digitized video data in 8-bit format will be output to the AvBus connector via the 8-bit video bus (Vin_VPO_[0:7]). ITU-R BT 656 4:2:2 YUV (YCbCr) format video will be output 8 bits parallel via Vin_VPO_[0:7] with clocking provided by the 27MHz line-locked clock (Vin_LLC_27.0MHz). This

clock is furnished to the AvBus connector for Host usage. Additionally, Vin_LLC_27.0MHz is coupled to the LLC input of the SAA7121H digital video encoder to synchronize its encoding operation.

Refer to the Philips SAA7113H data sheet Table 4 for output configuration and usage information. It is assumed that normal operation will be Data Type 15 (4:2:2 YUV (YCbCr) 8-bit format video). This is the standard ITU-R BT.656 data format that will also be input to the SAA7121H Digital Video Encoder (see 3.2.3). Figure 4 depicts this data format.

3.1.2 OmniVision OV6630AA CMOS CIF-Resolution Camera Module

The Host will provide (via the AvBus connector) an ITU-R BT.656-compatible interface to an OmniVision OV6630AA Color Digital Camera module for capturing QCIF/CIF-resolution color video. The OV6630 camera and lens combination is a separate assembly that will attach to the A/V module with a flat flexible cable via 32-pin header J12 (Table A-5). +3.3V power will also be supplied to the OV6630 via J12. The OV6630 will be programmed (via its I²C-like SCCB bus) by the Host. Details of OV6630 registers and settings may be found in the OV6630 data sheet.

While the OV6630AA module provides a 16-bit wide interface, due to AvBus pin limitations the upper 8 bits are ignored and the OV6630 will be operated in it 8-bit 4:2:2 Format mode (see OV6630 Data Sheet Table 4) with data transferred via CAMERA_Y[0:7]. Data sent via AvBus to the Host will be in the format | C_{bn} | Y_n | C_{rn} | Y_{n+1} |; where C_b, Y, and C_r are 8-bit quantities. The Horizontal reference signal from the OV6630 (CAMERA_HREF) is high during the active video region and may be used by the host to gate the capture of valid video and ignore blanked data.

CIF-resolution (352 pixels horizontally x 288 pixels vertically x 30Hz) video data captured locally by the OV6630AA is in the ITU-R BT.656 4:2:2 sampling format which may or may not require conversion to a different format (e.g., 4:2:0, 4:4:4, etc.) or a different color space (e.g., RGB). These conversions must be accomplished by the Host. As an example of Host processing, the OV6630 video input is driven by timing references produced by the video camera from a 12MHz master clock supplied by the FPGA; this timing source shall be repetitive and constant. Data from the video camera will arrive at a 30 frames-per-second (fps) rate (33.333ms/frame). This translates to 115.75us per line of video data for each of the 288 lines of a video frame. The Host data input from the Camera will be driven by two camera signals, CAMERA_VSYNC and CAMERA_HREF. CAMERA_VSYNC defines the beginning of a video frame (Line 1) and should cause the Host's horizontal line counter to be reset to zero. The Host must maintain a horizontal line count (e.g., 1 to 288), with this horizontal line count incremented (+1) on the rising edge of CAMERA_HREF. The high period of CAMERA_HREF encapsulates the video data and should cause the Host to store the line of video so it can be operated upon.

Note the above is for 352 x 288 x 30fps; other resolutions and frame rates will require a different clock and timing. Nominal register settings for CIF resolution at 30 frames per second are provided in Appendix B.

I²C (SCCB) address for the OV6630AA module is 0xC0 (write), 0xC1 (read).

3.1.3 Fujitsu MB86S02 CMOS CIF-Resolution Camera Module

The Fujitsu MB86S02 provides the same resolution as the OV6630 described above but requires an 18MHz clock from the Host. Connection of the MB86S02 module to the A/V module is via its 21-pin flexible cable inserted into ZIF connector J13 (Table A-6). Other than the 18MHz clock and the jumper setting differences described in section 3.1, above, the MB86S02 signals and timing are as described for the OV6630AA.

Nominal register settings for CIF resolution at 30 frames per second are provided in Appendix B. Note that these are the camera default settings and do not need to be initialized. I²C address for the MB86S02 are 0xC2 (write) and 0xC3 (read).

3.2 Video Output Processing

There are three forms of video output processing on the A/V Module; one to drive an analog RGB (e.g., VGA-resolution) monitor, one to drive a QVGA-resolution (Quarter-VGA) 320 x 240 RGB TFT LCD module, and another to output baseband video to an NTSC (or PAL) television monitor.

For a VGA monitor, RGB data is output from the Host in a 24-bit parallel format (8 bits each Red/Green/Blue) to the AvBus connector (DVD_R[0:7], DVD_G[0:7], DVD_B[0:7]). This data, along with clock, blanking and synchronization signals is furnished to a Analog Devices ADV7123KST140 triple 8-bit video DAC for conversion to analog. The analog RGB data with sync encoded on the Green channel is output to DB15 connector P1. The 24-bit RGB data bus (DVD_R[0:7], DVD_G[0:7], DVD_B[0:7]) is shared between the DAC and the 18-bit TFT LCD panel (J10), with only the six bits of each color used (DVD_R[2:7], DVD_G[2:7], DVD_B[2:7]). Unless it is intended to drive the monitor at the same timing and resolution (320 x 240) of the LCD panel, the DAC should be placed in its power-down mode by connecting jumper JT1 pins 1 – 2 when the LCD panel is being used. Conversely, the LCD panel should be disconnected from J10 when the Monitor is being used in a resolution/timing mode incompatible with the LCD panel.

Baseband composite video output may be achieved by the Host supplying ITU-R BT.656-compatible video to the Philips SAA7127H Digital Video Encoder. These interfaces are described in more detail below. Note that the processing described in subsequent sections is to show examples and is not meant to imply that this processing is done on the A/V Module.

3.2.1 RGB (Analog Monitor) Video Output Processing

Data input from the SAA7113H Video Input Processor is not compatible with the ADV7123 RGB DAC and must be converted to a compatible RGB format. As an example, ITU-R BT 656 compatible data input to the Host is in the 4:2:2 CbYCr luminance (Y) and color-difference (C_b , C_r) format. Since Cb and Cr samples are co-sited with even numbered luminance values, Cb and Cr values must be interpolated for the odd numbered luminance values. This provides a 4:4:4 CbYCr format that can easily be converted into the RGB color space and output to the ADV7123. Creation of the missing (odd) C_b , C_r values may be accomplished with simple replication, linear interpolation, or via a FIR filter. Note that the conversion processes must maintain the Y, C_b and C_r values within the limits defined in ITU-R BT.601-5 where:

$$16 \leq Y \leq 240$$

$$16 \leq C_b \leq 235$$

$$16 \leq C_r \leq 235$$

In this format, Cb and Cr are bipolar with zero equal to 128_{10} .

Conversion of the 4:4:4 $Y C_b C_r$ structure to RGB may then be done as follows:

$$R[i] = 1.164(Y[i] - 16) + 1.596(C_r[i] - 128)$$

$$G[i] = 1.164(Y[i] - 16) - 0.813(C_r[i] - 128) - 0.392(C_b[i] - 128)$$

$$B[i] = 1.164(Y[i] - 16) + 2.017(C_b[i] - 128)$$

Note that output to a standard VGA monitor requires progressive (non-interlaced) scan. If video is acquired from the SAA7113H for output via the ADV7123 to a standard monitor, it must be de-interlaced after RGB conversion and prior to being output to the ADV7123. Note also that synchronization and blanking signals that are monitor-compatible and not composite video-compatible must be generated for the ADV7123.

24-bit parallel RGB data is provided from the AvBus connector via DVD_R[0:7], DVD_G[0:7], DVD_B[0:7] to the ADV7123 triple video DAC for conversion to compatible analog video signals. Note that the ADV7123 can accept 10-bit R, G and B data but pin utilization of the AvBus connector limits this data path to 24 instead of 30 bits. The eight R, G and B data bits are provided to the eight most-significant bits of the ADV7123 RGB inputs with the two least-significant bits of each R, G and B held low.

Also provided by the Host to the DAC (via AvBus) are composite synchronization (DVD_CSYNC) and blanking (DVD_BLANK) signals. Vertical and horizontal synchronization signals (DVD_VSYNC, DVD_HSYNC) are available on the AvBus connector but are not used by the ADV7123. DVD_VSYNC and DVD_HSYNC are brought to pins 14 and 13 (respectively) of DB15 connector (P1) but are not required for a Sync-on-Green monitor. The analog RGB signals generated by the DAC are connected to P1 to drive an analog RGB monitor via a doubly terminated 75-ohm coaxial cable. The ADV7123 device internally encodes video synchronizing information onto the Green channel.

An oscillator provides a 25.175MHz clock to drive the ADV7123 Video DAC at VGA resolution with a 59.94Hz refresh rate; this same clock (VIDEO_CLK) is furnished to the AvBus connector for use by the Host. Alternatively, the oscillator may be disabled via jumper JP1 and the required clock furnished by the Host via the VIDEO_CLK line. Note that this oscillator may be replaced with a higher frequency oscillator (or the Host may furnish a higher-frequency clock) if higher resolution and/or refresh rates are desired. The 25.175MHz oscillator provides the required clocking for a 640 X 480 60Hz VGA monitor. This is determined as follows: Horizontal Lines (pixels) x Vertical Lines x Refresh Rate. Due to required overhead (e.g., horizontal and vertical retrace, etc), the 640 X 480 (viewable) display is actually 800 X 525 ($800 \times 525 \times 59.94 = 25.175\text{e6}$).

The (640 X 480 VGA-resolution) display is, essentially, a 480 row by 640 column matrix that is drawn one row at a time left to right, top to bottom. Upon reaching the right extremity (n, 640) the beam is blanked (turned off), returned to the left hand edge (horizontal retrace), and positioned to draw the next line. Upon reaching the bottom right extremity (480, 640) the beam is blanked and returned to the top left (0, 0) of the screen (vertical retrace). Additional (undisplayed) overhead associated with display timing increases the 640 X 480 display to 800 X 525 "pixel times". A 25.175MHz clock signal (CLK_MONITOR) will provide the required timing for the 640 x 480 display output (800 x 525) at a 59.94Hz refresh rate as follows:

Clock Frequency:	25.175MHz	(39.722ns)
Line Frequency:	31.469kHz	(31.778us)
Frame Frequency:	59.94Hz	(16.383ms)
One Line:	Front Porch:	8 pixels (0.318us)
	Horizontal Sync:	96 pixels (3.813us)
	Back Porch:	40 pixels (1.589us)
	Left Border:	8 pixels (0.318us)
	Video:	640 pixels (25.422us)
	Right Border:	8 pixels (0.318us)
	Total:	800 pixels (31.778us)
One Frame:	Front Porch:	2 lines (63.556us)
	Vertical Sync:	2 lines (63.556us)
	Back Porch:	25 lines (794.45us)
	Top Border:	8 lines (254.22us)
	Video:	480 lines (15.253ms)

Bottom Border:	8 lines	(254.22us)
Total:	525 lines	(16.683ms)

The 25.175MHz oscillator may be replaced with a higher frequency oscillator to support higher resolution monitors; e.g., VGA (640 x 480) @72 Hz requires 31.5MHz, SVGA (800 x 600) @ 72Hz requires 50.0MHz, XGA (1024 X 768) @ 75 Hz requires 78.75MHz, SXGA (1280 X 1024) @ 75Hz requires 135.0MHz. The ADV7123KST140 140MHz device furnished on the A/V Module is sufficient for SXGA resolution at 75Hz. If required, replacing the ADV7123KST140 with the 240MHz ADV7123KST240 device will accommodate higher resolutions.

3.2.2 LCD (RGB) Video Output Processing

Connector J10 (Table A-3) provides an interface to a Sharp LQ057Q3DC02 Color TFT LCD module. This 5.7 inch (diagonal) screen provides Quarter VGA (QVGA) resolution of 320 pixels horizontally and 240 lines vertically, which is different from the 352 x 288 CIF resolution data received from the OV6630 or MB86S02 CCD cameras or the 720 x 525 (NTSC) interlaced resolution data input from the SAA7113H.

Three zero-ohm jumpers, JT2, JT4 and JT5, configure the LCD display as follows:

JT2: connect pins 1:2 for VGA Timing, and 2:3 (default) for QVGA timing (see LQ057Q3DC02 data sheet)

JT4: connect pins 1:2 for Vertical reverse and 2:3 (default) for Vertical normal

JT5: connect pins 1:2 (default) for Horizontal normal and 2:3 for Horizontal reverse

The Host must provide the 6.144MHz clock for this interface (CLK_TO_LCD). This may be easily accomplished by dividing the 24.576MHz clock furnished to the Host via the AvBus by four and driving it out CLK_TO_LCD. This 6.144MHz clock factors to 375 horizontal pixel times, 256 vertical lines, with a 64Hz screen refresh rate. This provides a single horizontal line time of $61.035e^{-6}$ seconds and a frame time of $15.625e^{-3}$ seconds ($61.035e^{-6} \times 256$). Vertical and horizontal timings for this interface are:

Clock Frequency:	6.144MHz	(162.76ns)	
Line Frequency:	16.384kHz	(61.035us)	
Frame Frequency:	64.0Hz	(15.625ms)	
One Line:	Horizontal Sync:	16 pixels	(2.604us)
Front Porch:		32 pixels	(5.208us)
	Video:	320 pixels	(52.083us)
	Back Porch:	7 pixels	(1.139us)
	Total:	375 pixels	(61.035us)
One Frame:	Vertical Sync:	3 lines	(183.106us)
	Front Porch:	12 lines	(732.422us)
	Video:	240 lines	(14.648ms)
	Back Porch:	1 line	(61.035us)
	Total:	256 lines	(15.625ms)

A horizontal video line (LCD_ENAB held low) will begin with an active-low 16-clock (2.604^{μ}) horizontal synchronization pulse (LCD_HSYNC) followed by 32 clocks (5.208^{μ}) of "front porch" (clock only, no data). Following this, and coincident with the rising edge of the 49th clock, data enable (LCD_ENAB) will be brought high and kept high for the next 52.083^{μ} seconds (320 clocks), going low at the rising edge of the 321st (369th) clock. During this time the nth line of RGB data will be output on the upper 6 bits of the R, G and B (DVD_R[2:7], DVD_G[2:7] and DVD_B[2:7] data buses (LCD_R[0:5], LCD_G[0:5], LCD_B[0:5] to the LCD). The clock signal CLK_TO_LCD output from the Host to the LCD is the 6.144MHz clock. RGB data from the Host is latched into the LCD display on the rising edge of CLK_TO_LCD; consequently, data will be output on the RGB buses on the falling edge of the previous clock. At the rising edge of the 321st (369th) clock, LCD_ENAB is brought low. This is followed by 7 clocks (1.1139^{μ}) of "back porch" (clock only, no data); this is the end of the video line (375 clocks), and the next clock begins the output of video line n+1 from the Host.

Vertical timing is specified in horizontal line times, where one line time is equal to 61.035^{μ} ($375 \times 162.76^{\mu}$). The vertical frame begins with a 3-line period (183.106us) active low vertical sync pulse (LCD_VSYNC), followed by a 12-line period (732.422us) "front porch". During these 3 and 12-line periods only the 6.144MHz clock (375 clocks per line) and LCD_VSYNC are sent to the display with LCD_R[0:5], LCD_G[0:5], and LCD_B[0:5] held low. Following this, 240 lines of active video are sent as described above. A single line (375 clocks) "back porch" with the RGB data lines held low completes the vertical frame.

An ERG 8M052322 DC to AC Inverter provides power for the LCD backlight with the duty cycle fixed by a jumper on the inverter module. The jumper may be removed and the duty cycle (brightness) controlled by the Host via the LCD_PWM signal from the AvBus connector to inverter header J3 (see Table A3A).

3.2.3 Composite Video (CVBS) Output Processing

A Philips SAA7121H Digital Video Encoder provides conversion of ITU-R BT 656 4:2:2 (YCbCr) digital video signals (see Figure 3-1) to a baseband composite video (CVBS) and "S-Video" (Y/C) signals for output on RCA jack J2 (CVBS) and mini-DIN connector JR2 (Y/C). 5MHz analog low-pass filters are provided on the CVBS and the Y/C outputs. Timing for the SAA7121H is provided (when the SAA7113H is being utilized to capture video) by the SAA7121H's 27MHz Line-Locked clock (Vin_LLC_27.0MHz). Alternatively, if the SAA7121H is being used stand-alone, a 27.0MHz oscillator (U9), provides the required clocking. This same clock (27MHz_CLK) is furnished to the AvBus connector for use by the Host. Alternatively, U9 and U10 may be disabled using jumper JP3 to allow the Host to provide the required clock.

The 27MHz line-locked clock output from the SAA7113H video capture device is coupled to the line-locked clock (LLC) input of the SAA7121H by zero-ohm resistor R29. Operation in this mode allows the Host to retrieve BT.656-compatible data from the SAA7113H and route it to the SAA7121H via the AvBus connector and the digital video bus DV_OUT[0:7] with no additional processing. This mode also requires that the Real Time Control Input (RTCI) pin of the SAA7121H be coupled to the Real Time Control Output (RTCO) pin of the SAA7113H. This is accomplished through zero-ohm resistor R28. If this mode is used, zero-ohm resistor R26 must be removed to isolate the 27MHz oscillator from the SAA7121H and R27 must be populated in order to place the SAA7121H oscillator input at ground level. The A/V Module is shipped with this configuration.

The SAA7121H may be operated in either master or slave mode with each mode requiring different video synchronization schemes. In the slave mode the Host must generate the synchronization signals and provide these signals at the SAA7121H RCV1 (DV_RCV1) and RCV2 (DV_RCV2) pins. Refer to the

synchronization section of the SAA7121H data sheet for further details. Alternatively, the SAA7121H may be configured to synthesize timing and synchronization from an ITU-R BT 656-compatible data stream at the DV_OUT[0:7] port. It is assumed that this will be the normal mode of operation. In master mode the SAA7121H generates synchronization signals and furnishes them via the RCV1 (DV_RCV1) and RCV2 (DV_RCV2) pins.

Due to pin limitations on the AvBus connector Teletext capability is not available.

Nominal I²C register settings for ITU-R BT.656 operation in NTSC mode are provided in Appendix B. Zero-ohm jumper JT3 selects the SAA7121H I²C address as follows:

JT3 pins 2:3 (default) selects 0x88 (write), 0x89 (read)

JT3 pins 2:3 selects 0x8C (write), 0x8D (read)

3.3 Audio CODEC

A Philips UCB1400 stereo 20-bit Audio CODEC is used to provide stereo line-level and monophonic microphone input and stereo line-level/headphone out functions for the A/V Board. 3.5mm audio jacks provide input/output connectivity as follows:

J6: Stereo line-level out

J7: Stereo line-level in

J8: Mono microphone in

J7 and J8 are AC-coupled to the UCB1400; AC coupling of J6 is not required because of the UCB1400's virtual ground output to J6. Note that 2.5V electret cartridge bias is provided via an external voltage divider network; this bias voltage is blocked from the UCB1400's microphone input by the AC coupling.

Interface between the Host and the UCB1400 is via the AvBus connector, with the Host communicating with the UCB1400 via an AC97 interface. The UCB operates in master mode; with the Host operating as an AC97 controller device; in this mode the UCB1400 provides AC97 timing (Bit Clock). Details of the operation of the AC97 interface are somewhat complex and beyond the scope of this document. Refer to the UCB1400 data sheet and the AC97 Specification Rev. 2.1 for further details.

A 24.576MHz clock is provided to the UCB1400 from the same oscillator and clock distribution network that drives the SAA7111A video input processor.

3.4 Ancillary Functions

There are a few miscellaneous functions contained on the A/V Board that are not directly related to video or audio; these functions are described below.

3.4.1 Touchscreen Interface

Touch Panels are assumed to be resistive and will be processed on the A/V Module by the Philips UCB1400 CODEC (U15) that also contains a touchscreen controller. Digitally encoded position data will be transferred to the Host via the AC97 interface. X and Y touch screen inputs are provided to U15 via 4-pin header J11 (Table A-9). An interrupt signal (IRQ_OUT) can be generated to the Host to indicate a touch panel entry was made. U15's touch screen controller allows the measurement of X/Y positional information as well as pressure and plate resistance measurements.

3.4.2 Miscellaneous I/O

The UCB1400 CODEC provides ten general-purpose I/O bits that may be set/read via the AC97 interface. Additionally, four analog voltage inputs may be multiplexed into the UCB1400's 10-bit A/D converter. The 10 GPIO bits are connected to Header J4 (Table A-7) and the four analog voltages are input via Header J5 (Table A-8).

3.4.3 Keyboard/Mouse Interface

A SNCBTLV3125 quad FET Bus Switch interfaces standard PS2 keyboard and mouse connectors (JS1, JS2) to the FPGA via AvBus signals KBDATA, KBCLK and MSDATA, MSCLK. No processing of keyboard/mouse inputs is provided on the A/V Module.

4.0 A/V Module Power

The only power source available to the A/V Module is the +3.3VDC and +5VDC from the AvBus connector. Jumper JP6 will select either +3.3VDC or +5VDC to power the ADV7123 triple video DAC; the default setting is +3.3V. +5V is used to drive the LCD backlight inverter via J3.

The A/V Module will draw a maximum of 320ma @+3.3V from the AvBus connector with no LCD panel or CCD camera attached. The LQ057Q3DC02 LCD panel will draw a maximum of 160ma @+3.3V if attached. The ERG 8M052322 LCD backlight inverter will require approximately 900ma @+5VDC when attached. Addition of the OV6630AA module will draw an additional 20ma @+3.3V; the MB86S02 module will draw approximately 11ma @+2.8V. +2.8V power is derived from the +3.3V rail by an ADP3300 linear regulator; this +2.8V also powers a 74VCX162244 buffer providing +3.3/+2.8V translation for MB86S02 signals.

5.0 AvBus Connectors

High-density connector pads are located on the top (P2) and bottom (J9) of the module to provide a means for high-speed board-to-board communication. The signal connections on the top connectors are mirrored on the bottom connectors for board stacking and expansion capabilities. Table A-1 lists the signal names and pin connections for P2, and Table A-2 for J9

6.0 JTAG

There is no usage of JTAG on the A/V Module. JTAG connections on the AvBus connectors P2 and J9 are connected together for pass-through. These same JTAG connections are interfaced to header JP5 on the A/V Module (see Table A-4).

APPENDIX A

Connector Pinouts

Signal Name	Connector Pin #	Connector Pin #	Signal Name
+5V	1	71	DVD_B0
DVD_G0	2	72	GND
DVD_G1	3	73	DVD_B1
GND	4	74	DVD_B2
DVD_G2	5	75	GND
DVD_G3	6	76	DVD_B3
GND	7	77	DVD_B4
DVD_G4	8	78	+3.3V
DVD_G5	9	79	DVD_B5
GND	10	80	DVD_B6
DVD_G6	11	81	GND
DVD_G7	12	82	DVD_B7
+5V	13	83	DVD_R0
DVD_BLANK	14	84	GND
DVD_CS	15	85	DVD_R1
GND	16	86	DVD_R2
DVD_HS	17	87	GND
DVD_VS	18	88	DVD_R3
GND	19	89	DV_RCV1
CAMERA_CLK	20	90	+3.3V
CAMERA_HREF	21	91	DV_RCV2
GND	22	92	IRQ_OUT
CAMERA_VS	23	93	GND
CAMERA_PCLK	24	94	ADC_SYNC
+5V	25	95	DVD_R4
Vin_SCL	26	96	GND
Vin_SDA	27	97	DVD_R5
GND	28	98	DVD_R6
Vin_LLC_27.0MHz	29	99	GND
unused	30	100	DVD_R7
GND	31	101	AC97_SDATA_OUT
CLK_24.576MHz_B	32	102	+3.3V
Vin_RT	33	103	AC97_SDATA_IN
GND	34	104	AC97_BIT_CLK
KBCLK	35	105	GND

**Table A-1: P2 Pinout
(Top AvBus Connector)**

Signal Name	Connector Pin #	Connector Pin #	Signal Name
KBDATA	36	106	AC97_SYNC
+5V	37	107	AC97_RESET#
MSCLK	38	108	GND
MSDATA	39	109	Vin_VPO_0
GND	40	110	Vin_VPO_1
Vin_CE	41	111	GND
DV_OUT_RST#	42	112	Vin_VPO_2
GND	43	113	Vin_VPO_3
VIDEO_CLK	44	114	+3.3V
unused	45	115	CAMERA_RESET
GND	46	116	CAMERA_FODD
unused	47	117	GND
LCD_ENAB	48	118	Vin_VPO_4
+5V	49	119	Vin_VPO_5
CLK_TO_LCD	50	120	GND
Vin_RTS0	51	121	Vin_VPO_6
GND	52	122	Vin_VPO_7
Vin_RTS1	53	123	GND
27MHz_CLK	54	124	DV_OUT_7
GND	55	125	DV_OUT_6
DV_OUT1	56	126	+3.3V
DV_OUT0	57	127	DV_OUT_5
GND	58	128	DV_OUT_4
LCD_PWM	59	129	GND
CAMERA_Y0	60	130	DV_OUT_3
+5V	61	131	DV_OUT_2
CAMERA_Y1	62	132	GND
CAMERA_Y2	63	133	CAMERA_Y5
GND	64	134	CAMERA_Y6
CAMERA_Y3	65	135	GND
CAMERA_Y4	66	136	CAMERA_Y7
GND	67	137	PRI_TMS
PRI_TDO	68	138	+3.3V
PRI_TCK	69	139	PRI_TDI
GND	70	140	PRI_TRST#

Table A-1: P2 Pinout, Continued

Signal Name	Connector Pin #	Connector Pin #	Signal Name
+5V	1	71	DVD_B0
DVD_G0	2	72	GND
DVD_G1	3	73	DVD_B1
GND	4	74	DVD_B2
DVD_G2	5	75	GND
DVD_G3	6	76	DVD_B3
GND	7	77	DVD_B4
DVD_G4	8	78	+3.3V
DVD_G5	9	79	DVD_B5
GND	10	80	DVD_B6
DVD_G6	11	81	GND
DVD_G7	12	82	DVD_B7
+5V	13	83	DVD_R0
DVD_BLANK	14	84	GND
DVD_CSNC	15	85	DVD_R1
GND	16	86	DVD_R2
DVD_HSYNC	17	87	GND
DVD_VSYNC	18	88	DVD_R3
GND	19	89	DV_RCV1
CAMERA_CLK	20	90	+3.3V
CAMERA_HREF	21	91	DV_RCV2
GND	22	92	IRQ_OUT
CAMERA_VSYNC	23	93	GND
CAMERA_PCLK	24	94	ADC_SYNC
+5V	25	95	DVD_R4
Vin_SCL	26	96	GND
Vin_SDA	27	97	DVD_R5
GND	28	98	DVD_R6
Vin_LLC_27.0MHz	29	99	GND
unused	30	100	DVD_R7
GND	31	101	AC97_SDATA_OUT
CLK_24.576MHz_B	32	102	+3.3V
Vin_RTCD	33	103	AC97_SDATA_IN
GND	34	104	AC97_BIT_CLK
KBCLK	35	105	GND

**Table A-2: J9 Pinout
(Bottom AvBus Connector)**

Signal Name	Connector Pin #	Connector Pin #	Signal Name
KBDATA	36	106	AC97_SYNC
+5V	37	107	AC97_RESET#
MSCLK	38	108	GND
MSDATA	39	109	Vin_VPO_0
GND	40	110	Vin_VPO_1
Vin_CE	41	111	GND
DV_OUT_RST#	42	112	Vin_VPO_2
GND	43	113	Vin_VPO_3
VIDEO_CLK	44	114	+3.3V
unused	45	115	CAMERA_RESET
GND	46	116	CAMERA_FODD
unused	47	117	GND
LCD_ENAB	48	118	Vin_VPO_4
+5V	49	119	Vin_VPO_5
CLK_TO_LCD	50	120	GND
Vin_RTS0	51	121	Vin_VPO_6
GND	52	122	Vin_VPO_7
Vin_RTS1	53	123	GND
27MHz_CLK	54	124	DV_OUT_7
GND	55	125	DV_OUT_6
DV_OUT1	56	126	+3.3V
DV_OUT0	57	127	DV_OUT_5
GND	58	128	DV_OUT_4
LCD_PWM	59	129	GND
CAMERA_Y0	60	130	DV_OUT_3
+5V	61	131	DV_OUT_2
CAMERA_Y1	62	132	GND
CAMERA_Y2	63	133	CAMERA_Y5
GND	64	134	CAMERA_Y6
CAMERA_Y3	65	135	GND
CAMERA_Y4	66	136	CAMERA_Y7
GND	67	137	PRI_TMS
PRI_TDO	68	138	+3.3V
PRI_TCK	69	139	PRI_TDI
GND	70	140	PRI_TRST#

Table A-2: J9 Pinout, Continued

Signal Name	Pin #	Pin #	Signal Name
GND	1	17	DVD_G6
CLK_TO_LCD	2	18	DVD_G7
DVD_HSYNC	3	19	GND
DVD_VSYNC	4	20	DVD_B2
GND	5	21	DVD_B3
DVD_R2	6	22	DVD_B4
DVD_R3	7	23	DVD_B5
DVR_R4	8	24	DVD_B6
DVD_R5	9	25	DVD_B7
DVD_R6	10	26	GND
DVD_R7	11	27	LCD_ENAB
GND	12	28	+2.8V
DVD_G2	13	29	+2.8V
DVD_G3	14	30	R/L
DVD_G4	15	31	U/D
DVD_G5	16	32	V/Q
		33	GND

**Table A-3: J10 Pinout
(LCD Panel)**

Signal Name	Pin #
+5V	1
GND	2
LCD_PWM	3

**Table A-3A: J3 Pinout
(LCD Panel Backlight)**

Signal Name	Pin #	Pin #	Signal Name
n/c	1	2	PRI_TMS (SEC_TMS)
GND	3	4	PRI_TCK (SEC_TCK)
n/c	5	6	n/c
PRI_TRST# (SEC_TRST#)	7	8	PRI_TDI (SEC_TDI)
+3.3v	9	10	PRI_TDO (SEC_TDO)

**Table A-4: Header JP5
(JTAG)**

Signal Name	Pin #	Pin #	Signal Name
CAMERA_Y1	1	2	CAMERA_Y0
CAMERA_Y3	3	4	CAMERA_Y2
CAMERA_Y5	5	6	CAMERA_Y4
CAMERA_Y7	7	8	CAMERA_Y6
CAMERA_RESET	9	10	PWDN
CAMERA_FODD	11	12	Vin_SDA
CAMERA_HREF	13	14	Vin_SCL
CAMERA_VSYNC	15	16	GND
CAMERA_PCLK	17	18	GND
+3.3V	19	20	CAMERA_CLK
+3.3V	21	22	GND
n/c	23	24	n/c
n/c	25	26	n/c
n/c	27	28	n/c
n/c	29	30	n/c
GND	31	32	GND

**Table A-5: J12 Pinout
(OV6630AA Camera Module)**

Signal Name	Pin #	Pin #	Signal Name
CAMERA_CLK	1	12	PCLK
CAMERA_RESET	2	13	GND
CAMERA_PWDN	3	14	+2.8V
D0	4	15	Vin_SCL
D1	5	16	Vin_SDA
D2	6	17	n/c
D3	7	18	AVH
D4	8	19	VD
D5	9	20	GND
D6	10	21	+2.8V
D7	11		

**Table A-6: J13 Pinout
(MB86S02 Camera Module)**

Signal Name	Pin #
I/O 0	1
I/O 1	2
I/O 2	3
I/O 3	4
I/O 4	5
I/O 5	6
I/O 6	7
I/O 7	8
I/O 8	9
I/O 9	10

**Table A-7: J4 Pinout
(UCB1400 GPIO Signals)**

Signal Name	Pin #
AD0	1
AD1	2
AD2	3
AD3	4

**Table A-8: J5 Pinout
(UCB1400 GP A/D Inputs)**

Signal Name	Pin #
TSPY (Y+)	1
TSMY (Y-)	2
TSMX (X-)	3
TSPX (X+)	4

**Table A-9: J11 Pinout
(UCB1400 Touchscreen Inputs)**

APPENDIX B

SAA7121H I2C Register Settings for Operation in ITU-R BT.656 NTSC Mode

I2C Hex Address	Register Hex Value	I2C Hex Address	Register Hex Value
26	00	6B	00
27	00	6C	F9
28	19	6D	00
29	1D	6E	B0
3A	13	6F	14
5A	88	70	80
5B	76	71	E8
5C	A5	72	10
5D	2A	73	54
5E	2E	74	03
5F	2E	75	03
61	15	76	06
62	3F	77	10
63	1F	78	05
64	7C	79	10
65	F0	7A	18
66	21	7B	38
67	55	7C	10
68	56	7D	00
69	67	7E	00
6A	58	7F	00

NOTE: Registers not specified in this table should be initialized to '00'. Refer to SAA7121H data sheet.

**SAA7113H I2C Register Settings for
Operation in ITU-R BT.656 NTSC Mode**

I2C Hex Address	Register Hex Value	I2C Hex Address	Register Hex Value
01	08	43	FF
02	C0	44	FF
03	33	45	FF
04	00	46	FF
05	00	47	FF
06	E9	48	FF
07	0D	49	FF
08	88	4A	FF
09	01	4B	FF
0A	80	4C	FF
0B	47	4D	FF
0C	40	4E	FF
0D	00	4F	FF
0E	01	50	FF
0F	2A	51	FF
10	40	52	FF
11	80	53	FF
12	B7	54	FF
13	01	55	FF
14	00	56	FF
15	00	57	FF
16	00	58	00
17	00	59	54
18 To 1E	00	5A	0A
20 To 3F	00	5B	83
40	02	5C To 5D	00
41	FF	5E	00
42	FF	5F	00

**OmniVision OV6630 I2C Register Settings for
Operation in 8-bit ITU-R BT.656 Mode
320 x 288 x 30fps**

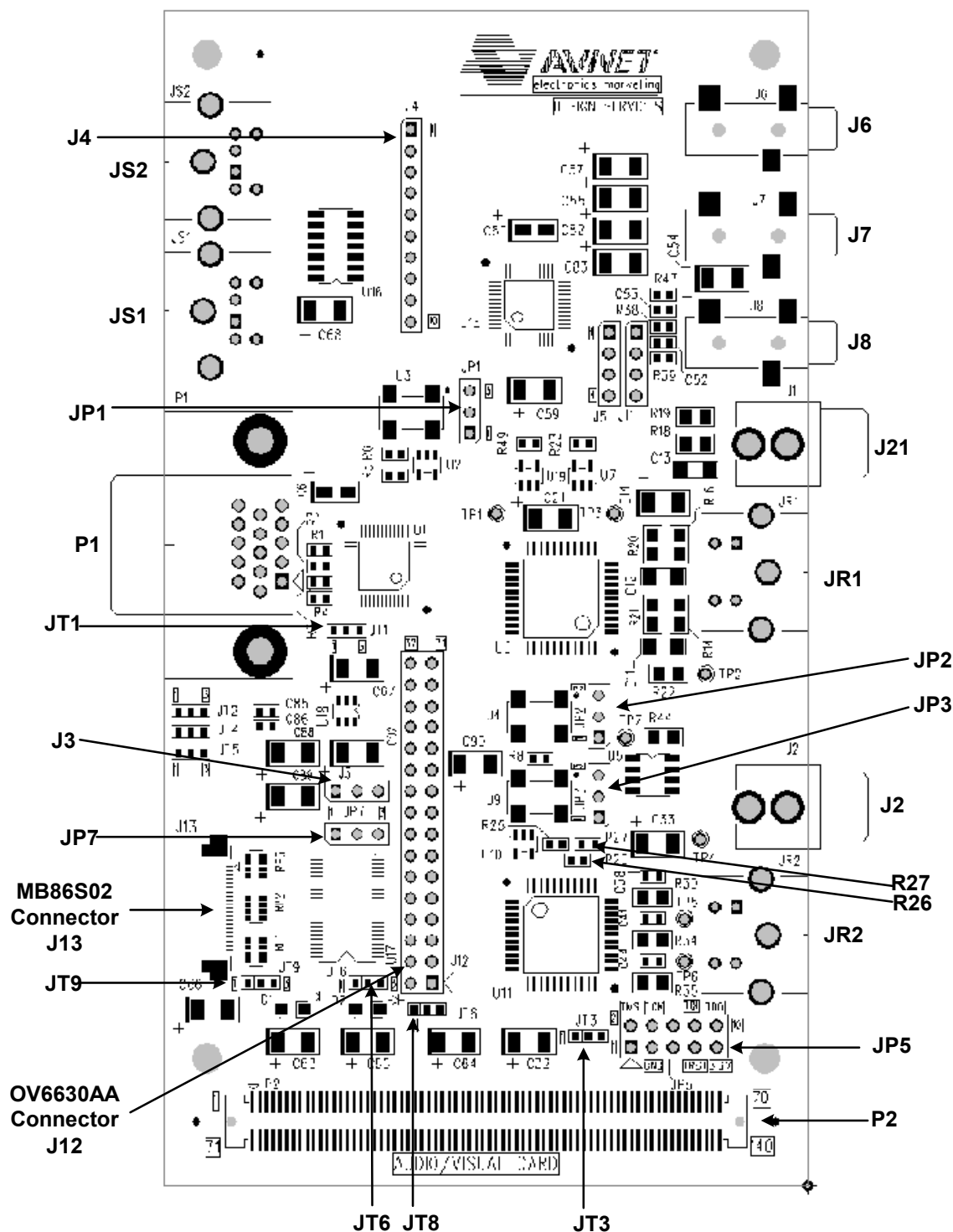
I2C Reg. Address	Register Hex Value	I2C Reg. Address	Register Hex Value	I2C Reg. Address	Register Hex Value
12	80	21	10	40	00
03	C0	22	88	41	00
04	4E	23	C0	42	80
05	0F	24	43	43	3F
06	80	25	8A	44	A0
07	8D	26	B2	45	20
08	7E	27	A6	46	20
09	4E	28	02	47	00
0A	7F	29	00	48	7F
0B	FF	2A	00	49	00
0C	20	2B	00	4A	00
0D	24	2C	A0	4B	00
0E	20	2D	85	4C	D0
0F	15	2E	86	4D	10
10	4E	2F	7E	4E	A0
11	01	30	4E	4F	07
12	34	31	4E	50	FF
13	21	32	2F	51	7F
14	04	33	26	52	FF
15	01	34	03	53	4E
16	03	35	4E	54	23
17	38	36	8F	55	CC
18	EA	37	80	56	12
19	04	38	83	57	F1
1A	93	39	80	58	75
1B	00	3A	0F	59	01
1C	7F	3B	3C	5A	2C
1D	A2	3C	1A	5B	0F
1E	C4	3D	80	5C	10
1F	04	3E	80	5D	4E
20	20	3F	0E	5E	4E

**Fujitsu I2C Register Settings for
Operation in 8-bit ITU-R BT.656 Mode
320 x 288 x 30fps**

I2C Reg. Address	Register Hex Value	I2C Reg. Address	Register Hex Value	I2C Reg. Address	Register Hex Value
01	00	23	0F	47	00
02	00	24	B4	48	80
03	00	25	00	49	80
04	00	26	00	4A	02
06	0D	27	6E	4B	02
07	B0	28	CE	4C	40
08	08	29	66	4D	00
09	A0	2A	7E	4E	00
0A	00	2B	E1	4F	E0
0B	00	2C	00	50	1A
0C	00	2D	FF	51	F0
0D	00	2E	00	52	06
0E	33	2F	FF	53	1B
0F	07	30	00	54	CA
10	80	31	FF	58	00
11	80	32	1D	59	31
12	80	33	1B	5A	2E
13	00	34	BC	5C	08
14	33	35	00	5D	2D
15	07	36	0F	5E	00
16	26	37	40	5F	02
17	F0	38	95	60	00
18	EA	39	01	61	00
19	CC	3A	0C	62	02
1A	3C	3B	10	63	00
1B	F8	3C	78	64	68
1C	EB	41	00	65	00
1D	00	42	25	66	04
1E	15	43	8A	67	00
20	7F	44	1D	69	2E
21	7F	45	1B	6A	47
22	7F	46	BC		

APPENDIX C

Top of A/V Module



Bottom of A/V Module

